Implementation of a Novel architecture for VLSI testing

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Abstract—**Time, power, and data volume are among some of the most challenging issues for testing System-on-Chip (Soc.) and have not been fully resolved, even if a scan-based technique is employed. A novel architecture, referred to the Selective Trigger Scan architecture, is introduced in this paper to address these issues. This architecture reduces switching activity in the circuit-under-test (CUT) and increases the clock frequency of the scanning process. An auxiliary chain is utilized in this architecture to avoid the large number of transitions to the CUT during the scan-in process, as well as enabling retention of the currently applied test vectors and applying only necessary changes to them. It also permits delay fault testing. Using ISCAS 85 and 89 benchmark circuits, the effectiveness of this architecture for improving Soc. test measures (such as, time, and data volume) is experimentally evaluated and confirmed.**

Keywords—Scan test, test data volume, test application time, test power, test compression, delay testing.

I INTRODUCTION:

Intellectual property (IP) cores are commonly used for designing a System-on-Chip (Soc.). Although IP cores can help to reduce the design cycle time, they still pose many challenges when testing is considered. The pre-computed test patterns that are provided by core vendors must be applied to each core within the power constraints of the whole Soc. As a system integrator may use a core in different platforms with diverse test mechanisms (whether for on-chip or off-chip implementation), the test mechanism of the core must take into account issues related to data volume, application time, and power consumption durintest. Moreover, other models (such as for delay faults) must be considered to improve the overall test quality. A comprehensive solution is very difficult; such a solution major changes in different parts of the design as provided by the IP providers. Power and test data volume are especially challenging:

II PREVIOUS WORKS

Recent years have seen the development of many techniques for overcoming the aforementioned difficulties in VLSI testing. In this section, some of these works are briefly reviewed.

Power reduction: Circuits are often designed to operate in two modes: normal and test modes. The test mode usually dissipates more power than the normal mode, especially if a scan mechanism is employed.

During the data scan-in process, the difference between two adjacent bits moves through the scan path due to the shift operation; many floating transitions are then applied to the CUT. Fig. 1 shows this process for shifting the ak vector ðak;0; ak;1; ak;2; ak;3; ak;4Þ when the ak_1 vector is in the scan chain; (1) can be used to determine the number of shift-in transitions:

Many techniques in the technical literature have been proposed to reduce the number of these transitions for power dissipation management.

III A SELECTIVE TRIGGER SCAN ARCHITECTURE FOR VLSI TESTING

Scan cell values during shift operation. Being all active at the same time, only a fraction of the scan cells is active in each test clock cycle. Bhunia have proposed a solution to reduce test power by inserting blocking logic into the stimulus path of the scan flip-flops to prevent propagation of the scan ripple effect to logic gates. Ghosh describe a technique for minimizing power dissipation during scan testing. For a given set of test vectors, the (local) optimal reordering of the scan cells is found to minimize a score function; the selected function is a linear combination of power and area overhead. The scan cell reordering technique in uses a heuristic algorithm to modify the order of the scan cells within the chain to reduce switching activity. Chen has presented an integrated approach to reduce both power consumption and test application time. This method is made possible by combining scan architecture and several other techniques, including scan cell and vector reordering. Test time. In a scan tree design, the chain is divided into multiple scan chains and a cell may drive multiple scan cells. This technique is suitable for test time reduction. In this scheme, the same test data is stored in different scan chains; however, this method suffers from reduced controllability in the design. The effectiveness of scan tree architecture depends on the correlation between test data in the structure of the scan tree. Bonhomme have proposed scan tree architecture for reducing test application time. This technique is based on a dynamic reconfiguration mode, allowing a reduction in the dependence between a test set and the final scan tree architecture.

This procedure does not require additional test control inputs and an MISR is used for circuit response compaction. Miyase have proposed a scan tree method for multiple scan inputs; in a multiple scan design, the number of

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scan trees is equal to the number of scan inputs. As each scan input drives a scan tree, then test data volume and the scan tree of maximum height dominates application times. They have also proposed a method for test compression in multiple scan designs.

IV OUR CONTRIBUTIONS

This work proposes a novel scan architecture that is referred to as the Selective Trigger Scan Architecture (STSA). This scan architecture uses a triggering (enabling) chain in addition to the data registers. Furthermore, triggering chain hardware is designed to take advantage of similar adjacent data for test compression. Instead of shifting new serial data into the data registers, the triggering chain decides where a data flip-flop must toggle or retain its old value. Retaining data causes a small number of transitions at the data register outputs and low power dissipation.

Along with test reformatting techniques, this Architecture can reduce test time and power. It can also reduce data volume by enabling the application of compression algorithms on its reformatted data. This structure can be used as a core or chip-level design-fortest (DFT) technique. In addition, it is applicable to delay fault testing. When applied at the core level, substantial improvements in power and test time can be achieved by reformatting the precomputed vectors rather than starting with a new set of tests.

V THE PROPOSED ARCHITECTURE

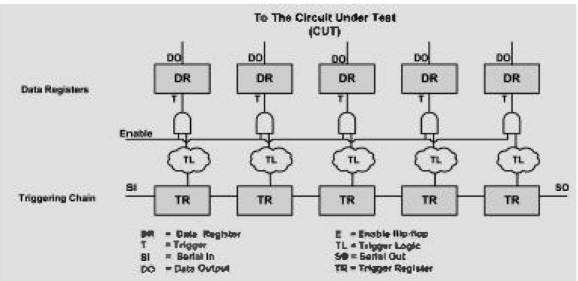

Fig 1 . Proposed scan-chain architecture.

We start explanation of our proposed architecture with a simple example. Let us assume thatV1 is an existing test vector in a scan chain and V2 is the next test vector that must be shifted. Comparing V1 and V2 transitions, there are only three differences in their bits that are called necessary transitions. If we were to use a standard scan chain and shift V2 into the scan chain in eight test clocks, with each shift, transitions would occur. For example, shifting the rightmost 1 of V2 into the scan chain causes five transitions in the eight scan flip-flops. All together, shifting V2 would cause 32 transitions that are called unnecessary transitions. On the other hand, parallel loading V2 directly into our architecture eliminates unnecessary transitions on the input of a CUT.

Hence, our scan architecture should eliminate the Operation of the circuit. The proposed architecture serves two purposes. One is to reduce the activity at the data outputs and the second is to facilitate test data compression. This architecture has data registers that contain the test data applied to the CUT, a triggering chain where the test data is shifted in, and a triggering logic circuit with an enabling AND that determines how the test data should be decoded and trigger the data registers. The triggering chain is for reducing the activity at the data register outputs. For this purpose, instead of shifting test vectors into the data registers, triggering data is obtained by formatting test vectors and shifted into the triggering chain. For example, if the triggering logic has an identity function, the current data register is 00101110, and the new test vector is 01100111, then the triggering chain must contain 01001001, that is, the bitwise difference of the two vectors. This architecture also blocks changes in the test data from being directly applied to the CUT. The

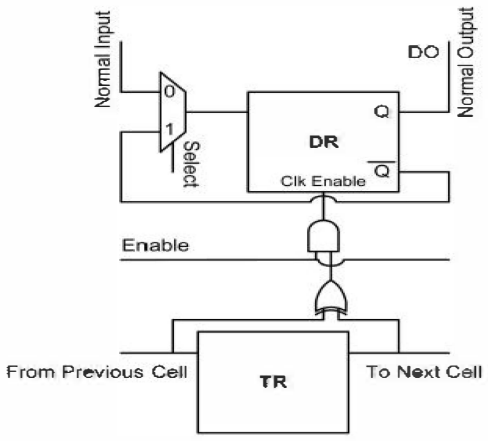

Fig. 2. Scan cell structure of the proposed scan architecture.

triggering logic comes into play for compression of test data. For test compression, instead of shifting the difference of consecutive test vectors into the triggering chain, the 0! 1 and 1! 0 transitions of the difference are shifted. An XOR gate implements the triggering logic. The structures of a scan cell of the proposed scan chain. In this case, for the two aforementioned test vectors, 01101101 should be shifted into the triggering chain. This is formed by the XOR of adjacent bits of the difference vector 01001001, starting from the right-hand side.

The DR flip-flops is the main storage cell and contains the vector that must be applied to the CUT. The TR chain provides the data required for selective triggering. Testing starts by resetting the DR chain. The TR chain cell has three modes of operation: Shift, Trigger, and Normal. The Shift and Trigger modes are used for testing,

This requires n scan clocks. After n clocks in the Shift mode, the cell enters the Trigger mode for a single clock. In this mode (based on the TR chain data), some of the DR flip-flops inverts their values to obtain the new vector. A test vector is reconstructed in a single test cycle (Fig. 6 shows this process).

As the Enable signal can be generated internally, no additional pin is required. This signal can be easily generated through a pulse after receiving n clock cycles. Moreover, the Select signal of the MUX does not require an additional pin; the same signal in conventional scan chains can be used to determine the Test and Normal modes. In the Test mode, the Select signal selects the 1 input of the MUX (from the Q output), while, in the normal mode, it selects the other input (which directs the Normal Input to the input of the DR flip-flop). Therefore, the proposed STSA requires no additional test pin compared to conventional scan structures. The output response is not captured in the scan chain; however, there are many techniques available in the current literature that can be used at no loss of coverage depending on the application and

its constraints. Significant improvements to Soc. testing are achieved using the proposed architecture; these improvements are described in more detail here.

VI EXPERIMENTAL RESULTS

The proposed architecture has been evaluated using fully specified vectors generated for some of the ISCAS 85 and 89 benchmark circuits. The full-scan versions of the sequential benchmark circuits and predefined fully specified test vectors are utilized. Shows the number of necessary and unnecessary transitions for the application of the test sets to the circuit inputs.

TTB denotes the total number of unnecessary transitions in the scan chain. TNB and TNA denote the number of necessary transitions required for the application of thsame test vectors to the inputs of the CUT before and after vector reordering, reordering algorithm. In some cases, scan vector reordering significantly affects the number of transitions.

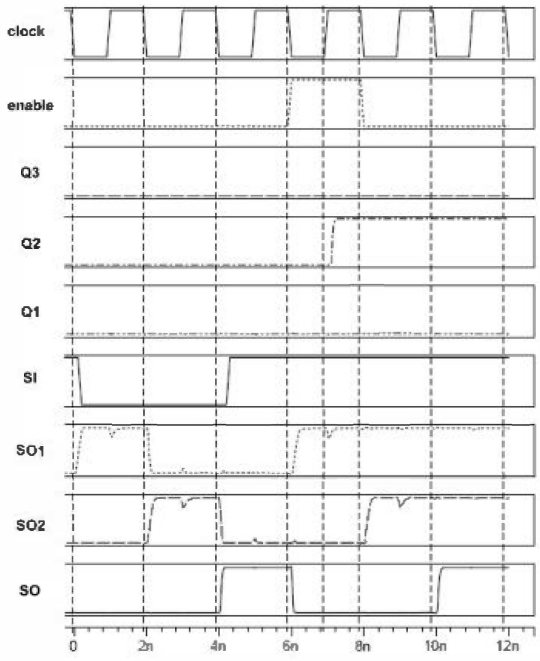

Fig. 3. SPICE simulation of the proposed scan chain.

The test vectors are reordered to reduce the number of transitions between vector pairs; this is accomplished by constructing a complete graph with test vectors as nodes and the Hamming distance between the two connected vectors as the weight of the edge between two nodes.

VII CONCLUSIONS

This paper has proposed a novel scan architecture that considerably improves SoC testing in terms of power and time. Power consumption is reduced during the test process by preventing transitions in the scan chain from spreading into the CUT. Data in this architecture is scanned at higher clock frequencies because no MUX is introduced in the critical scanning path. It was shown that the proposed architecture can also be used for reconstructing the original test vectors from their differences within a compressed data stream. The applicability of the proposed architecture to compression leads to a shorter test time and reduces ATE memory requirements. A further feature of this Architecture is its Comparing Necessary Transitions and Unnecessary Transactions Runtime of the reordering with respect to the number of test vectors in each benchmark circuit.

Applicability to delay fault testing: This is achieved by enabling the application of two arbitrary test vectors to the CUT in two consecutive clock cycles. The process of test data reformatting for this new architecture has been presented; a Golomb-like coding compression algorithm has been proposed and analyzed. Experimental results for various ISCAS benchmark circuits have confirmed the Effectiveness of the proposed approach on predefined fully specified vectors. When embedded in a core by the provider, an integrator for different scan-based strategies in testable SoC designs can use this architecture.

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