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Customized Power Grid Solutions for Mitigating IR Drop and Noise in Advanced Process Nodes

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***Abstract* -- As semiconductor technology advances into lower nodes such as 7nm and below, power integrity and power consumption have become critical concerns in digital VLSI design. One of the key contributors to power inefficiencies and reliability issues in these nodes is the degradation of the Power Grid due to increased current densities and limited routing resources. This paper presents the importance of Power Grid optimization as a fundamental step toward achieving power-efficient designs in lower technology nodes. It highlights the significant role of Power Grid enhancement during the Floor planning stage, where early architectural decisions can influence the performance and integrity of the entire power delivery network (PDN). By incorporating intelligent power strap planning, early IR-drop and electromigration (EM) analysis, and layout-aware power grid synthesis, it is possible to reduce dynamic and static power losses while improving voltage stability across the chip. The proposed methodology demonstrates measurable improvements in power delivery efficiency and design reliability, making it a crucial consideration in next-generation system-on-chip (SoC) implementations. This can be achieved by understanding the routing resources available, complexity of the design and its requirements. Power Grid improvement, shielding of the clock nets to mitigate noise and signoff checks are explored in this work.**

Keywords: Physical design, Power Distribution Network, IR Drop and Electromigration

I. INTRODUCTION

Power consumption is a key concern in today's electronic devices. In modern era, reduced power consumption aids to improve battery life, reduce heat generation, and greater environmental sustainability.PPA analysis assesses power usage at various stages of chip operation from idle states to peak performance - to ensure efficient power management. In physical design, to improve the overall power supply of the design the power grid plays a major role. The goal of Power Planning is to satisfy the power requirements of the design, being robust and to meet the EMIR during Signoff. Power Grid if not robust will fail EMIR checks and it will cause the chip to fail. So, the grid should be robust enough for proper power supply and helps the EMIR closure during signoff. In higher technologies power was not as critical as in lower technologies. In higher nodes the size of the transistor is large, and the density is less with low leakage, so power is not critical whereas lower nodes the size of the transistors is small, and the density is high in the same area with more leakage operating at higher frequency, so power becomes a major bottleneck for performance and reliability of the chip. So, a robust power grid helps in the overall power improvement of the chip and mitigating IR drop.

II. OBJECTIVE

To perform PnR [Place and Route] with the synthesized netlist, constraints and pushdown collaterals. Build the Power Grid, validate at PnR tool and run the PnR. Validate the PG grid by running signoff checks. If there are any issues found, reiterate the process till an optimal grid is achieved.

III. LITERATURE SURVEY

Vidhi Gandhi, Yashvi Patel, Bhavesh Soni, Gaurav Joshi. "Power Budget Improvement Using Floorplan Methodologies in Lower(28nm) Technology Node", in 2023 IEEE International Symposium on Smart Electronic Systems (iSES), 18 December 2023 – 20 December 2023. [1]

The growing demand for compact, power-efficient, and high-performance devices has driven advancements in integrated circuit (IC) technology. As a result, the ASIC industry is shifting to smaller technology nodes to meet performance and space constraints. Floorplanning is a critical phase in physical design, directly influencing performance, area, and power integrity. It involves the strategic placement of I/O pads, macros, and power-ground networks, with a major focus on reducing routing congestion. The study evaluates three floorplanning approaches - Data Flow Analysis (DFA), Pin Placement, and Hierarchical Design at the 28nm node using industrystandard tools. Results show that Pin Placement delivers the best performance, with 52% lower IR drop than Hierarchical and 73% better than data flow analysis.

Vishant Gotra, Srinivasa Kodanda Rama Reddy, Tanniru Srinivasa Rao, Pavithra P." Optimized Power Grid Planning for Enabling Low Power Features for Leakage.Power Reduction in SOC", in 2020 IEEE 33rd International System-on-Chip Conference (SOCC),08 September 2020 – 11 September 2020. [2]

The dual challenges of leakage power reduction and Power Delivery Network (PDN) integrity are paramount in modern VLSI design. Multiple Power Pin (MPP) standard cells offer significant leakage savings retaining data even when logic is powered down, but their extensive use demands a backup supply grid that strains routing resources, worsens congestion, and risks IR-drop violations. The study introduces an optimized, verification-driven backup-grid planning methodology that enables high-frequency, high-utilization MPP deployment without timing or convergence penalties. Applied to a 28 nm SoC, the approach delivers ≈ 20 % leakage reduction via auto power-gating, with no added IR-drop or layout-closure issues, and can be seamlessly integrated during ECO phases.

Tsu-Wei Tseng, Chang-Tzu Lin, Chia-Hsin Lee, Yung-Fa Chou, Ding-Ming Kwai." A power delivery network (PDN) engineering change order (ECO) approach for repairing IR-drop failures after the routing stage", in Technical Papers of 2014 International Symposium on VLSI Design, Automation and Test, 28 April 2014 - 30 April 2014. [3]

PDN evaluation and synthesis techniques are invaluable during early physical design but often become impractical after routing, when scarce routing resources demand a targeted repair strategy. Traditional fixes such as indiscriminate wire widening or density increases ignore signal routing constraints and can exhaust remaining routing channels, complicating later ECO efforts. To address this, we introduce a signoff-stage PDN repair flow based on a Greedy-Pareto-Optimal (GPO) algorithm that pinpoints the most impactful regions for power-rail reinforcement. By balancing IR-drop improvement against routing-resource consumption, our GPO-driven ECO was integrated into the PnR tool and, on an image-signal-processor test case, cut worst-case IR-drop from 9.34% to 3.84% (a 58.9% gain) using wires pitched at 3.5× the minimum routing pitch

C. -J. Lee, S. S. -Y. Liu, C. -C. Huang, H. -M. Chen, C. -T. Lin and C. -H. Lee, "Hierarchical power network synthesis for multiple power domain designs," Thirteenth International Symposium on Quality Electronic Design (ISQED),19 March 2012 – 22 March 2012. [4]

The study automates synthesis and optimization of power-delivery networks for designs with multiple power domains. It begins with an architectural model that integrates sleep transistors and maps the network to an RC circuit via Modified Nodal Analysis, solved efficiently using the Conjugate Gradient Method. To enforce IR-drop limits, a Simulated Annealing–based optimizer minimizes total power-stripe area under a specified IR constraint. Power domains are organized in a tree structure, enabling recursive, hierarchical optimization for each domain. Fully integrated into the EDA flow. The approach was validated on both industrial SoCs and MCNC benchmarks, yielding a 31–35% reduction in P/G network area while keeping worst-case IR-drop below 10%

H. T. Chen, H. -L. Lin, Z. -C. Wang and T. Hwang, "A new architecture for power network in 3D IC," 2011 Design, Automation & Test, 14 March 2011 -18 March 2011. [5]

Through-silicon vias (TSVs) enable high-density vertical interconnects in 3D ICs, dramatically shortening global wiring lengths. However, widespread TSV adoption is impeded by IR-drop, thermal-dissipation, per-pin current-delivery limits, and the need to support multiple voltage domains. To address these challenges, a Stacked-TSV and Power-Distributed Network (STDN) architecture that integrates power delivery, thermal management, and decoupling capacitance into a unified framework. The STDN establishes low-impedance current paths to minimize IR drop, enhances heat extraction to lower peak temperatures, and embeds distributed decoupling capacitors to suppress supply-noise, all while alleviating IO power-pin constraints. Validated on MCNC benchmarks for both single- and multi-domain designs, STDN achieves superior 3D floorplanning efficiency, reduces worst-case IR drop and thermal hotspots, lowers power-supply noise, and shrinks both die area and total signal-wire length.

IV. COMPONENTS IN THE DESIGN

The key physical components inside the design are Standard cells, Macros, Physical Cells, Power Delivery Network, Clock Tree and I/O Ports.

A. *Standard Cells*

Standard cells are the basic building blocks of complex designs. These cells are designed and verified functional blocks used in a physical design which can be reused across various designs. Standard cells are made of transistors. They maybe of the following types.

• Logic gates – AND, OR, NAND, NOT, NOR, XOR.

• Sequential elements – Flops and Latches.

• Combinational cells – Mux, Adders, Subtractors and Comparators.

Standard cells are characterized with different threshold voltages to balance the designs power, performance and area. They can be classified as below.

• HVT cells – Slow speed and low leakage power which are used in less critical paths.

• SVT cells – Balanced performance and leakage power which are used generally.

• LVT cells – High speed and more leakage power which are used in critical paths.

• ULVT cells – Very high speed and significantly more leakage power which are used in high-speed circuits.

B. *Macros*

Macros are small pre-designed reusable designs which are larger than standard cells but smaller than entire chip which have a specific function. It can be simply called as a mini-chip inside the chip. These are well optimized designs in terms of PPA and provided by vendors. They also have fixed I/O ports. They can be classified as below.

• Hard macros – Design layout is fixed both logically and physically like SRAMs, PLL, ADC etc.

• Soft macros – Flexible and Synthesizable like ALU, FFT etc.

• Firm macros – Implemented partially and balances flexibility like specialized DSP blocks etc.

C. *Physical Cells*

Physical cells don't have any specific logical functionality in the design. They help to meet the electrical and physical requirements of the design based on the design rules from the technology PDKs. They can be classified as below.

• Tap Cells – Prevent latch-up violations in the design ensuring the n-well continuity in the design.

• Filler Cells – Fills the gap between standard cells to prevent base DRC violations.

• Boundary Cells – Dummy cells placed at the start and end of the row to prevent the cell damages during fabrication and also ensures proper n-well termination.

• Antenna Cells – Diodes inserted for long wires protects the design from antenna effects by collecting the charges and safely discharging them during fabrication.

• Spare Cells – Additional logic gates and sequential cells inserted throughout the design uniformly which can be used for ECO's without doing a full PnR and signoff cycle again.

D. *Power Delivery Network*

Power Delivery Network ensures that all the cells in the design get a stable and uniform power and ground supply by using power ground rails, stripes and rings. Higher and wider metal wires are used to ensure a robust power supply. The PDN network is built from the topmost layers to the bottom most layer ensuring connectivity to the standard cell power pins.

E. *Clock Tree*

The clock tree helps the clock signal to reach all the sequential elements of the design and tries to ensure that the clock reaches simultaneously to all the elements with minimum skew and latency. The clock tree network consists of clock ports, clock gates, clock muxes, clock buffers, clock inverters and the flops.

F. *IO Ports*

The I/O ports are interface between the design to other designs within the chip or to the outer world elements. The functionality of the I/O ports may be configured as data, clock, reset, control, ground and power. They can be classified as follows.

• Input Ports – receive data from outside the design.

• Output Ports – sends data from the chip to outside.

• Bidirectional Ports – sends and receives data.

• Power and Ground Ports – deliver and return the power.

V. PHYSICAL DESIGN FLOW

The steps in physical design are represented in the below flow diagram. Power planning is elaborated in the flow diagram

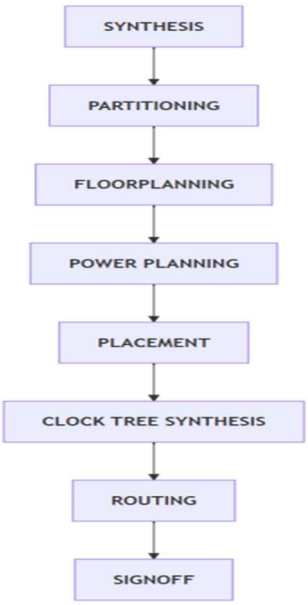

Fig 1. Physical Design Flow Diagram

A. *Synthesis*

As shown in Fig 1 Synthesis is the process of converting synthesizable RTL code into simplified and optimized gate level netlist which is used during PnR implementation. It optimizes the design based on the constraints and improves the overall PPA of the design. Scan insertion happens during synthesis which converts to normal flops to scan flops which makes the design testable after fabrication. Synthesis is of two types.

• Logical Synthesis – More abstract and ensures design functionality and meet timing targets.

• Physical Synthesis – Consider the physical input from floorplan and does better optimization in terms of PPA.

B. *Partitioning*

As shown in Fig 1 Partitioning is the backbone of physical design. It is the process of dividing a large complex design into smaller sub blocks without affecting the functionality of the original design. It helps to improve the overall turn around for the design implementation, better handling of the designs and to improve PPA. The partitioning can be based on functional, physical or power.

C. *Floorplanning*

As shown in Fig 1 Floorplanning is an important step in the PnR implementation. A good floorplan helps to achieve a better PPA whereas a bad floorplan degrades the PPA and makes the implementation difficult. The inputs of the floorplan are Netlist, Scan DEF, SDC from synthesis, LEF and LIB from the technology vendors and DEF [size and shape with port placement] from the chip level. It involves creating the floorplan with the given dimensions, creating rows, placing physical cells [endcaps and well taps], placing I/O ports and placing macros.

D. *Power Planning*

As shown in Fig 1 Power planning is the step where the power and ground is distributed uniformly and reliably to all the standard cells, macros and other IPs in the design through the Power Distribution Network (PDN). The PDN network has the rails, stripes, power rings, power pads and bumps which helps to distribute the power from the source to the cell. The power planning may also be termed as power network synthesis, and it is routed before clock and signal routing as it carries the higher importance. Estimation of the power drawn by the chip is critical in power planning. The goals of power planning are to provide proper power and ground connections to the cells, mitigate noise, IR drop, and to reduce electro migration effects. A reliable and stable power grid helps to improve the overall PPA.

E. *Placement*

As shown in Fig 1 The standard cells are placed in the design during this stage and optimization happens to meet the PPA requirements. In this stage redundant cells are removed from the design, high fanout data nets are being optimized to achieve better timing and area. After placement, we need to check for legalization issues, local hotspots, density, congestion, DRVs and timing.

F. *Clock Tree Synthesis:*

As shown in Fig 1 CTS is an important stage of the design where the clock is distributed to all the sequential elements from the clock port. The clock tree is built and optimized based on the constraints to meet the design requirements and to achieve a minimum latency and skew. It is the stage where the clock nets are routed. After CTS, we need to check whether the latency requirements are met, correct cell types are used in the clock paths, NDR is applied, setup and hold timing requirements and routing congestion.

G. *Routing*

As shown in Fig 1 Routing is the stage where the signals are routed, and timing optimization happens. This is the final stage before signoff checks. It ensures that all the pins are connected, there are no opens and shorts, minimum wirelengths, no detours, meet the setup and hold timing requirements.

H. *Signoff Checks*

As shown in Fig1 The signoff consists of STA, LEC, PV, and PGV as the major steps. During STA timing is checked for the design and if any violations is there timing ECOs are implemented. The cycle is repeated till the timing is met. LEC is checked on the post route database and also after each ECO to ensure the proper functionality of the design. During PV the design is checked for DRC, LVS, Antenna and ERC checks. PGV is the step where the design is checked for static, dynamic violations, signal EM and power EM violations. The design can only be closed if STA, LEC, PV and PGV are clean.

VI. IMPORTANCE AND ISSUES OF POWER GRID

As the technology node shrinks, the number of transistors in the chip increases exponentially. In modern chips, power consumption has become very critical as it needs to be more compact and energy efficient. The increase in power consumption in a device can be classified as static and dynamic power consumption.

• **Static power consumption** – Even when the chip is in idle state, the transistor consumes power, which becomes significant as the transistor size shrinks.

• **Dynamic power consumption** – Higher the number of transistors higher will be the switching activity resulting in more power consumption.

Issues:

The issues and ways to mitigate the issues in the power grid are as follows.

• **Voltage Drop** – The number of metal layers in the design increases as the technology shrinks. In the power supply network, we might see voltage reduction due to resistance in the wires. This may lead to functional failure of slowness as the transistors receive a reduced voltage. This can be improved by incorporating thicker metal layers and refining the power grid design, resulting in a more stable voltage throughout the design.

• **Ground Bounce and Noise** – Fluctuations in ground potential can be caused due to simultaneous switching of nearby circuits. Noise and instability in signal

transmission can affect the chip reliability. This can be resolved by even power distribution, and design with lower inductance in power lines.

• **Electromigration** – Higher current density causes gradual displacement of atoms in the device. Degradation of the routing might lead to broken connections and reduced the lifespan of the chip. Using of higher metal layers with better resistance or wider metal stripes helps to mitigate electromigration.

A. *Importance:*

The importance of a robust power grid in the design are as follows,

• Reliable Power Distribution throughout the design

• Mitigating Ground Bounce

• Power Integrity

• Stable voltage and reduced IR drop

• Better heat management and electromigration prevention

• Minimized power noise

• Improved chip lifespan and manufacturability

Structure, Improvement Strategies and Evaluation

The power grid structure consists of the following parts.

• **Power Pads** – This is a vital component of the Power Distribution Network (PDN). It consists of specialized I/O pads that supply power and ground to the chip. These pads serve as the connection point between the external power source and the internal power grid. Positioned along the chip's periphery and integrated into the pad ring, they help ensure consistent and reliable power delivery across the entire design.

• **Rings** – Metal loops that surround the core area of the design that carry power around the design. These are part of the power grid that connect the stripes to the pads. These can be classified as core power rings, I/O power rings and macro power rings.

• **Stripes** – Parallel metal wires running across the chip in both horizontal and vertical direction that carry power across the design. These are parts of the power grid that connect the rings and the rail.

• **Rails** - Horizontal or vertical conductive metal wires laid above the power and ground pins of the standard cells. These form the final level of power distribution in the hierarchy, connecting directly to the active components from the stripes

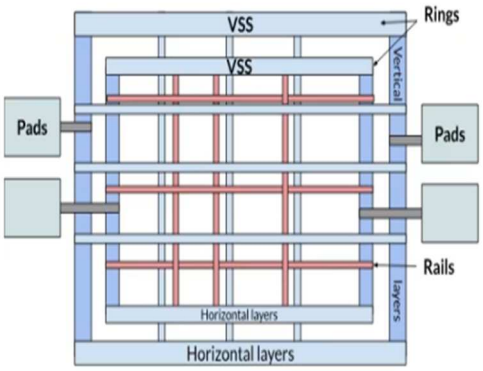

Fig 2. Structure of Power Grid

B. *Power Grid Improvement during Power Planning*

In Fig 2 The grid can be improved by upgrading the existing grid with a robust grid through an iterative process till the grid is robust to support the design requirements. As shown in Fig 3, Below are the steps that can be followed to improve the grid.

• Identify the supply requirements of the design like what is the operating voltage, how many power nets are there.

• Determine the grid topology what should be top PG layer to be used in block level, what should be the width spacing and set to set distance, whether the layer should be staple or stripe.

• Create power stripes in the top layers till it reaches the lower layer.

• Create a power rail in the lowest layer where the standard cell power pins are present to ensure connectivity between the power supply and standard cell pins.

• Run the PnR flow and evaluate the robustness of the grid by running EMIR analysis. Check for any DRC violations in the design by running PV checks. If any DRC or IR drop specific to a layer are observed repeat from step 2 by adjusting width, set to set distance and spacing till we meet the design requirements

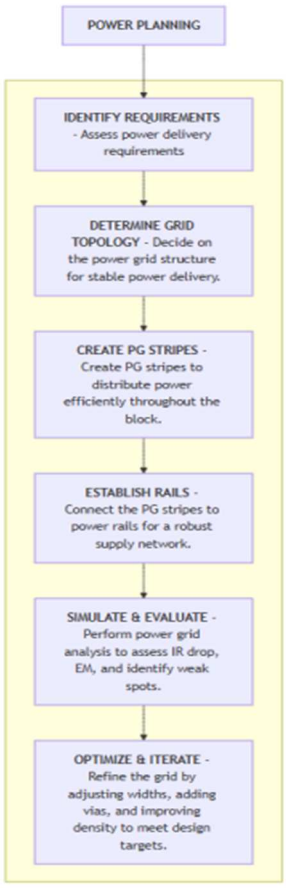

Fig 3. PG Grid Improvement Methodology during Power Planning

a) Addition of VIA0/M1/VIA1 after ECO

After the completion of the PnR and the ECO cycle in the final database, we will still observe there are tracks available to add PG in via0/metal1/via1. So, these vias are reinforced in the design through a script which significantly helped to improve the overall IR drop of the design as these connect to the standard cell power pins through rails.

b) Reinforce PG after ECO

After the completion of the PnR and the ECO cycle in the final database, we will still observe there are tracks available in the higher layers. By reinforcing PG in the higher layers helps to improve the overall PG grid strength and thus mitigating the IR drop.

c) Evaluation:

PNR Level Checks:

• The Power Grid should not have any opens.

• The Power Grid should not have any shorts.

• There shouldn't be any missing via's in the power grid at critical regions.

• The macro pins should be connected to the Power Grid.

• There should not be any PG grid related DRCs.

• Global nets should be defined properly to connect the PG nets to the standard cell pins.

C. SIGNOFF CHECKS

a) IR Drop Analysis

In a design the power is uniformly distributed through the metal layers and each metal layer has a specific resistance associated with it. Current flows through these metals when a voltage is applied, and a certain amount of voltage drop occurs due to the resistance of the metals and this drop in voltage is termed as voltage drop. This in turn results in increasing the delay causing timing violations and also induces noise degrading the performance.

The acceptable IR drop limit, the scenario it needs to be signed off, the dynamic runs will be vectored or vectorless and other factors are determined at the start of the project. For example, if a design is operating at 0.75V and the limit is 10% of the operating voltage the drop shouldn't fall beyond 0.675V. If the drop goes beyond the limit we need to fix it.

b) Static Drop Analysis

The drop is independent of cell switching that means the design is in idle state. In this case the drop is calculated with the help of metal's resistance value. Leakage current is dominant in this type of analysis. In a design the static IR drop must be always clean, and it will have a lower limit than dynamic run. The main cause for static IR drop is the resistance in the metal layers of the power grid and leakage currents from the standard cells in the design. This can be analyzed through EDA tools like Voltus or Redhawk. If there are static IR drop violations in the design, it can be fixed by using any one of the following strategies.

1. Increasing the width of the stripes.

2. Increase the number of PG wires in the design by changing the set-to-set distance and width.

3. Check if any via is missing in the design add more power vias.

4. Can also be fixed by controlling the VT utilization and type of cells used in the design

c) Dynamic Drop Analysis

The drop is calculated with the help of the switching of the cells. When a cell switches at the active edge of the clock, it demands a significant surge of current or voltage to

activate. However, voltage drops can prevent the cell from receiving adequate voltage, potentially pushing it into a metastable state, which can degrade timing and overall performance. This is time-dependent and harder to predict due to its reliance on real-time switching patterns. The analysis can be run in both vectored and vector-less. This can be analyzed through EDA tools like Voltus or Redhawk. If there are dynamic IR drop violations in the design, it can be fixed by using any one of the following strategies.

- Increasing the number of stripes.
- Adding DCAP cells around the violating cells.
- Spreading of the cells in violating area.

d) EM Analysis

Power EM occurs when a high current density flows through the power grid, causing metal ions to drift due to momentum transfer from electrons. Over time, this can create voids or hillocks. This affects reliability and reduces the life span of the chip. his can be analyzed through EDA tools like Voltus or Redhawk. If there are powerEM violations in the design, it can be fixed by using any one of the following strategies.

1. Widening of the stripes to increase via area to aid current distribution.

2. Adding additional stripes to increase the via area to ensure current distribution.

3. Spreading of the cells in the critical area to reduce the requirement of power.

e) PV Checks

Physical verification is an important stage in the signoff. The Design Rules for the technology are checked at this stage. The following are the important checks to check the PG grid.

- DRC

  DRC is the signoff check used for verifying the layout design against a set of design rules provided by the foundry. The rules specify constraints like minimum metal width, spacing between different layers, via dimensions, and layer overlap tolerances. Violations of these rules could lead to manufacturing defects and unreliable chip performance. These can be checked through EDA tools like Calibre. If any issue found in the PG grid it needs to be corrected by construction and should go through PnR cycle and run DRC check again to verify it is clean.

- LVS

  Layout versus Schematic is a verification process in VLSI design used to ensure that the physical layout of a chip matches its schematic. It ensures the integrity of the circuit before fabrication. If there are any PG grid shorts and opens in the design LVS will fail. The open or short maybe at the block level or at the top level or even during the integration of blocks in the top. If any issues are found it should be fixed and should check again to make the LVS clean.

The above is the signoff checks carried out by me after creating the PG grid and improved the robustness of the PG grid based on the results.

VII. DESIGN SPECIFICATION

The design uses 3nm technology at 1.2 GHz with 4M cells, 20 macros, 16 metal layers, and optimized dimensions (600 µm × 2500 µm) for 70% utilization

SL No	Technical parameter	
1.	Technology	3nm (Nano Meter)
2.	Operating Frequency	1.2GHz (Giga Hertz)
3.	Standard cell count	4 million
4.	Number of Macros	20
5.	Number of Ports	8451
6.	Number of Clocks	57
7.	Number of Metal layer	16
8.	Top PG layer	16
9.	Tools	Innovus, Calibre, PrimeTime and Voltus
10.	OS	Linux
11.	Block height	600um (Micro Meter)
12.	Block width	2500um (Micro Meter)
13.	Block Utilization	70%

Table 1. Technical Parameters of the Design

VIII. RESULTS

I have carried out several PG grid trials and based on each trials analysis have modified the grid structure to get the robust power distribution network and below is the comparison of the it to the existing grid. The Fig 4 summarizes PG grid trial results and highlights improvements in the modified grid for a robust power distribution network.

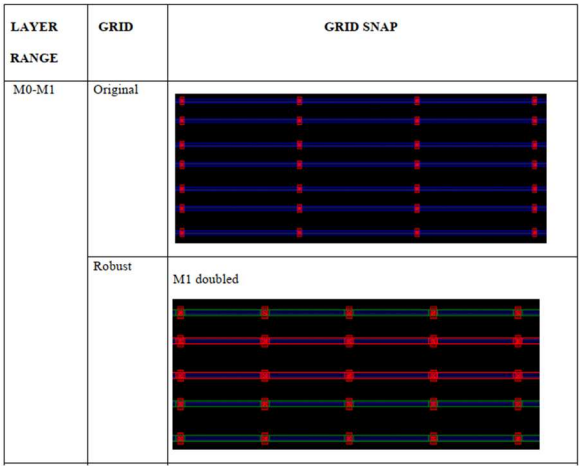

Fig 4. Comparison of Modified PG Grid Structure with Existing Grid

This table 2 presents the Quality of Results (QoR) metrics comparing the original power grid structure with the modified robust grid. Key improvements include reduced noise, enhanced power efficiency, and significant IR-drop reduction while maintaining clean LVS and antenna checks.

QoR Contents	Original Grid	Robust Grid
Timing	X	Similar to X.
Noise	408	251
Power	X	Improved by 5%
Utilization	X	Same as X.
DRC	85	97
PGV		
Static IR	4	Clean
Dynamic IR	X	Improved by 30%
Power EM	Clean	Clean
PV		
DRC	283	345
LVS	Clean	Clean
Antenna	Clean	Clean

Table 2. QoR Comparison Between Original PG Grid and Robust PG Grid

IX. CONCLUSION

After the successful creation of the robust PG grid after multiple trials following results can be observed.

• Timing remains Similar to the original grid run, indicating there is no impact and design can be successfully closed.

• Noise violations have significantly reduced from 408 to 251 due to the reduction of coupling capacitance between the nets. This helps in better DRV and timing closure during ECO implementation.

• The overall power consumption of the design has been improved by 5%. Since the design is replicated and used multiple times in the top level it helps in significant improvement of the overall power.

• The design utilization remains the same indicating that there is no congestion in the design due to the robust grid.

• The DRC in the design is increased from 85 to 97 compared to the original grid which are easily fixable.

• Static IR drop is clean with the robust grid where we observe 4 violations in the original grid.

• The overall dynamic IR drop violation count has improved by 30% with the robust grid which was the overall goal of the project. It helps in faster design closure and meeting the design requirements.

• Power EM is clean with both the grids ensuring that there are enough via tapping's and proper power supply to the instances.

• There is an increase in the calibre DRC count from 283 to 345 which can be easily addressed.

• LVS and Antenna violations are clean ensuring that there are no shorts or opens in the design.

• These results were in accordance with the detailed explanation of contents present in chapter.

X. ACKNOWLEDGMENT

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XI. REFERENCES

[1] Vidhi Gandhi, Yashvi Patel, Bhavesh Soni, Gaurav Joshi. "Power Budget Improvement Using Floorplan Methodologies in Lower(28nm) Technology Node", in 2023 IEEE International Symposium on Smart Electronic Systems (iSES), 18 December 2023 – 20 December 2023.

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[4] C. -J. Lee, S. S. -Y. Liu, C. -C. Huang, H. -M. Chen, C. -T. Lin and C. -H. Lee, "Hierarchical power network synthesis for multiple power domain designs," Thirteenth International Symposium on Quality Electronic Design (ISQED),19 March 2012 – 22 March 2012.

[5] H. -T. Chen, H. -L. Lin, Z. -C. Wang and T. Hwang, "A new architecture for power network in 3D IC," 2011 Design, Automation & Test, 14 March 2011 -18 March 2011.